Tallinn University of Technology

School of Information Technologies

**IAS0600 Digital Systems Design with VHDL**

Extended syllabus

Autumn 2022

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| **Course aims/objectives:** | The aim of the course is the introduction of the VHDL (Very High-Speed Integrated Circuit (VHSIC) Hardware Description Language) fundamentals, an overview of the reconfigurable systems on the example of FPGAs (Field Programmable Gate Arrays), and an introduction to the development flow for FPGAs. |
| **Learning outcomes:** | Having finished the subject, students will be able to:   * use state-of-the-art tools for FPGA programming; * understand how to describe basic digital logic elements using VHDL; * design a digital system based on its specification using VHDL; * simulate and test the designed system to verify that it works according to the specification; * analyze synthesis results. |
| **Brief description of the course (topics):** | Digital systems design using VHDL and FPGA. FPGA architecture. Synthesis process. Data types in VHDL. Signals and variables. Concurrent and sequential statements. Combinational and sequential logic elements. Synthesizable and non-synthesizable constructs. Modeling styles: dataflow, behavioral and structural architecture. Testbench and simulation. Finite State Machine (FSM) and datapath for algorithm implementation. |
| **Language of the course:** | English |
| **ECTS credits:** | 6 ECTS |
| **Students:** | This is an elective course for students studying in the IASM program. |
| **Special needs:** | Persons with disabilities can participate in this course. Please inform the professor(s) at the beginning of the course of any special instruction, or assessments of this course that may be necessary to enable you to fully participate in this course. |
| **Registration:** | Students who would like to take the course should declare the course in the ÕIS (Student Information System) by deadlines set in the academic calendar. |
| **Prerequisite courses and/or knowledge:** | No obligatory prerequisite courses. |
| **Professor(s):** | Natalia Cherezova, MSc, Early-stage researcher, [natalia.cherezova@taltech.ee](mailto:natalia.cherezova@taltech.ee). |
| **Contacting Professor(s):** | Preferred means of contact email, responses provided within two workdays. |
| **Schedule for classes:** | Classes take place every week on Wednesday, at 15:45-19:15, in ICT-501. |
| **Study process description:** | The course is practice-oriented. During the lectures, the material required to solve the labs is introduced. During the practice, students solve the lab tasks individually. For each lab, students write a report. |
| **Course’s e-support:** | Course materials can be accessed via the e-learning environment Moodle under the course title Digital Systems Design with VHDL <https://moodle.taltech.ee/course/view.php?id=31790>. Students can enroll in the course themselves using the **password: VHDL2022**. If you have no Moodle account yet, please create it by filling in the registration form at <https://moodle.taltech.ee/login/?lang=en>. |
| **Study literature:** | Volnei A. Pedroni, Circuit Design and Simulation with VHDL, The MIT Press, 2010.  Sarah L. Harris & David M. Harris, Digital Design and Computer Architecture, Elsevier, 2016. |
| **Continuous assessment:** | Students have to solve six labs throughout the course. Labs are done individually. Each lab should be presented to the instructor in the class. For each lab, students should write a report. |
| **Evaluation criteria for continuous assessment:** | Each lab gives 10 points. Up to 10 bonus points can be earned if the labs are finished in a timely manner. |
| **Exam:** | The exam is in the form of a written closed-book test. Students have 90 minutes to answer eight questions. The exam covers all the topics introduced during the course. |
| **Evaluation criteria for the exam:** | Up to 40 points. |
| **Final grade:** | Lab points (60) + exam points (40) + bonus points (10) = Total points  The sum of points for each item is converted into a grade using the following principles:  “5” excellent 91-100+  “4” very good 81-90  “3” good 71-80  “2” satisfactory 61-70  “1” poor 51-60  “0” fail less than 51 |
| **Academic integrity:** | As a student at Tallinn University of Technology, you have an obligation to conduct your academic work with honesty and integrity according to University standards. It is expected that all work that you submit will be your own and that you have actually done the work that you are submitting. Plagiarism and cheating will not be tolerated. Should you be found to be guilty of such activities, it will be followed with grade “0” for the assignment/exam and a notice will be filed to the School’s Committee for Handling Violations of Academic Practice and Contemptible Behaviour. Depending on the Committee’s proposal, it may lead to Dean issuing a letter of reprimand or in case of repeated or very severe misconduct, exmatriculation from the University. |

**Detailed schedule and topics**

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| Week | Lecture | Practice |
| #1 (31.08.22) | Course overview   * Topics * Hardware and software * Schedule * Labs overview * Report requirements * Grading system | — |
| #2 (07.09.22) | Introduction to VHDL   * Hardware description languages vs software programming languages * VHDL history * Synthesizable vs non-synthesizable * Types, objects, operators * Design entity | Lab tutorial 1   * Vivado overview * How to create a new project * Design sources * Testbench and simulation |
| #3 (14.09.22) | Introduction to FPGA   * Reconfigurable hardware * FPGA architecture * FPGA design flow | Lab tutorial 2   * Assertions * Synthesis and implementation |
| #4 (21.09.22) | Dataflow modeling style   * Modeling styles in VHDL * Dataflow modeling * Concurrent signal assignments * Assertions * Functions | Lab 1. 2-bit comparator |
| #5 (28.09.22) | — | Lab 1. 2-bit comparator |
| #6 (05.10.22) | Structural design   * Structural modeling style * Component instantiation * Type conversion | Lab 2. 2-bit adder |
| #7 (12.10.22) | — | Lab 2. 2-bit adder |
| #8 (19.10.22) | Behavioral modeling style   * Processes * Signals vs variables * Sequential statements * Sequential logic | Lab 3. Counter |
| #9 (26.10.22) | — | Lab 3. Counter |
| #10 (02.11.22) | (*No new topic is introduced in lab 4. It requires students to use the knowledge gained through the first three labs*.) | Lab 4. Creeping line |
| #11 (09.11.22) | — | Lab 4. Creeping line |
| #12 (16.11.22) | Parametric design   * Complex arithmetic circuits * Multiplicator model * Parametric design * Generate statement * Complex types | Lab 5. Parameterizable multiplier |
| #13 (23.11.22) | — | Lab 5. Parameterizable multiplier |
| #14 (30.11.22) | Finite State Machines   * FSM overview * FSM for hardware design * Datapath * FSM controller * Latch inference | Lab 6. Greatest common divisor |
| #15 (07.12.22) | — | Lab 6. Greatest common divisor |
| #16 (14.12.22) | — | Lab 6. Greatest common divisor |