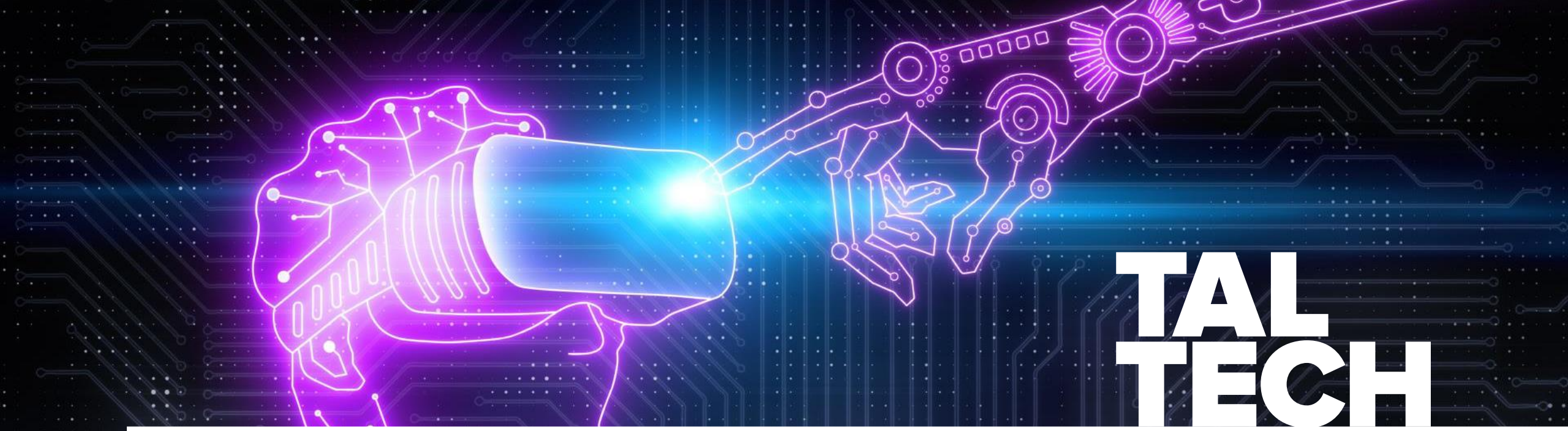


Microprocessor Systems Laboratory

Lab Assignment 1

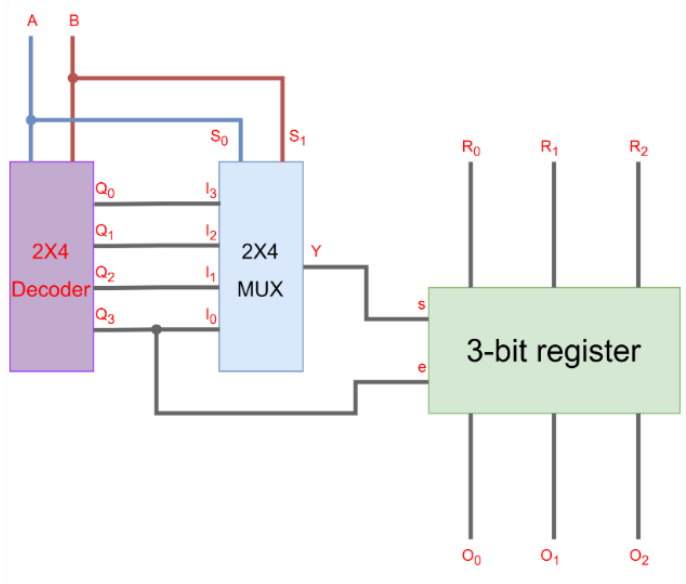
23.09.2022

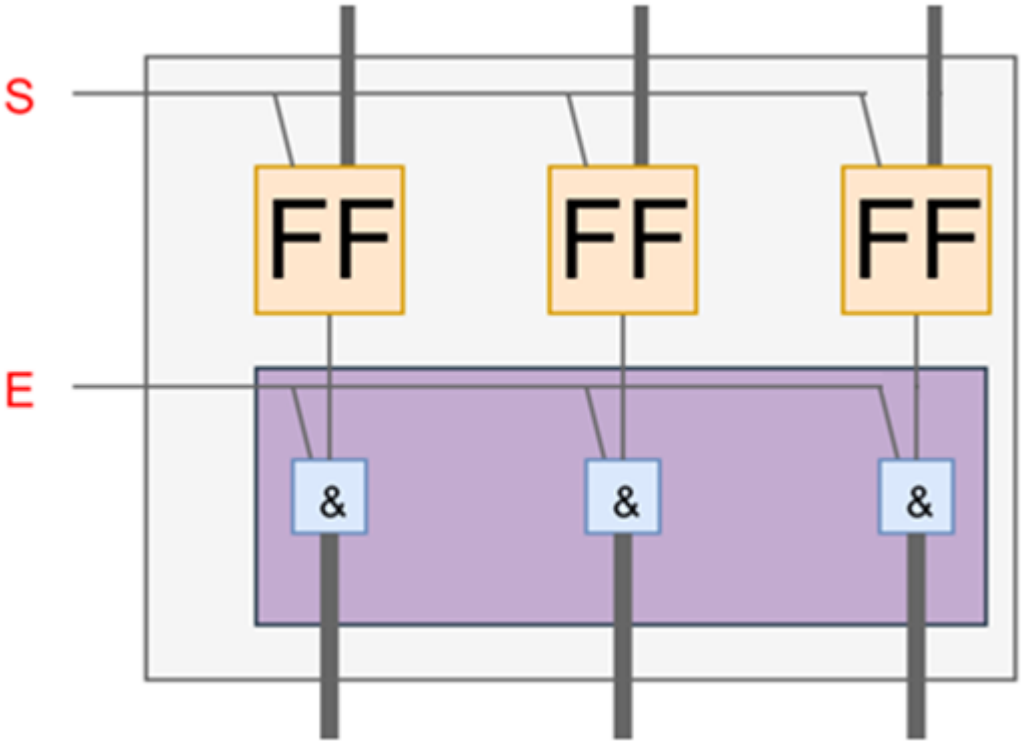
Lab Assignment 1- session 2

- Previous session:
  - Got started with LogiSim
  - Designed components for an ALU and a controller:
    - Subtractor (Half, full)
    - Comparator
    - Decoder (4x2)
    - Encoder (2x4)
    - MUX (4x1)

Lab Assignment 1- session 2

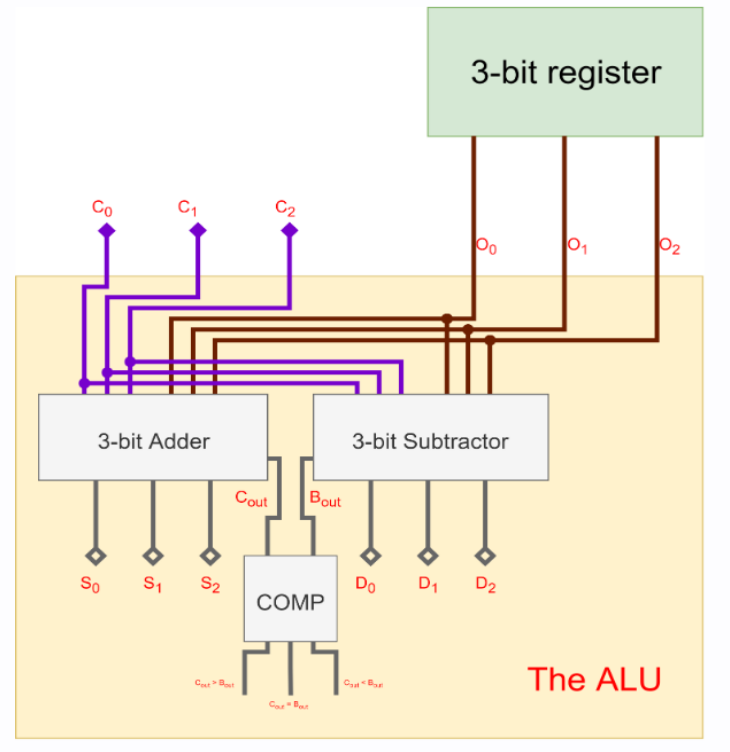
- This session:
  - Finish parts 1 and 2
  - Write the truth tables in a document file
  - Save each component separately
  - Start part 3-section 1:
    - Do Home Task 1, part 1, consider it as a Flip-Flop
    - Use it as FF for designing a 3-bit register



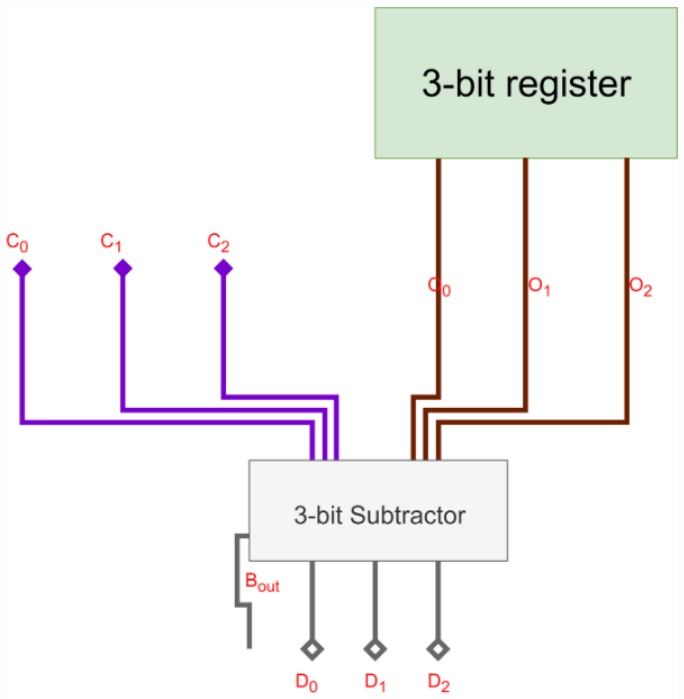


Lab Assignment 1- session 3

- This session:
  - Complete the part 3-section 1
  - Create the designs for part 3-section 2:



group1 (IASM)

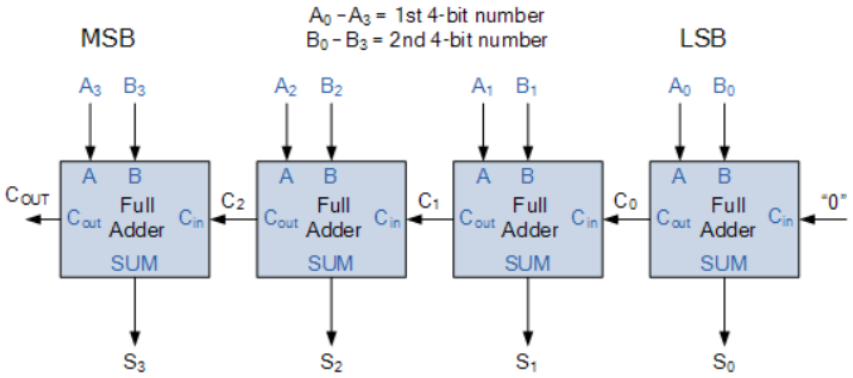


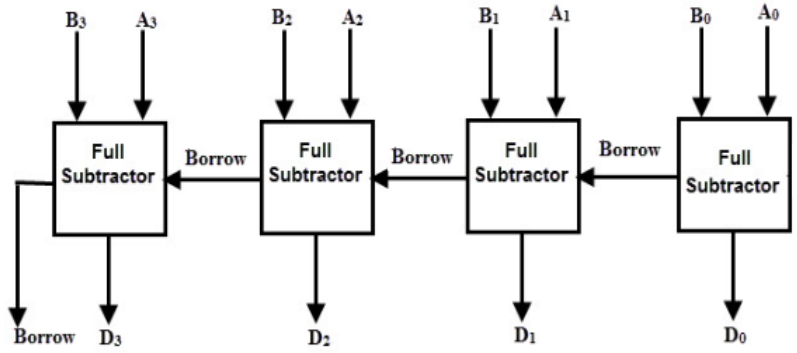
group2 (MAHM)

3-bit Full Adder and Subtractor

- Full Adder:
  - S = (A XOR B) XOR Cin
  - Cout = (A AND B) OR (A AND Cin) OR (B AND Cin)

- You have to create a 3-bit adder
- You have to create a 3-bit subtractor





THANKS FOR YOUR ATTENTION